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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/894,294	06/27/2001	Rajeev K. Nalawadi	42390P11478	7596

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EXAMINER
WANG, ALBERT C

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/894,294	NALAWADI ET AL.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Original claims 1-29 are presented.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-9, 11, 12, 14, 15, 17, 19, 24, 25, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi, U.S. Patent No. 6,615,288, in view of Chaiken, U.S. Patent No. 6,128,732.

As per claim As per claim 1, Herzi teaches a system comprising:

a processor coupled to a bus (Fig. 2, CPU 201);

a memory coupled to the bus (Fig. 2, memory 203);

an external bus controller coupled to the bus (Fig. 1, USB controller; Col. 2, 24-35); and

a basic input-output system (BIOS) coupled to the bus (Fig. 2, BIOS 202), the BIOS comprising an external bus support component to cause a interrupt to be generated and to provide support for external bus enabled devices responsive to the interrupt (Col. 5, lines 36-52; Figs. 3 & 4).

However, Herzi does not expressly teach generating the interrupt periodically. Chaiken teaches generating a periodic interrupt and providing support for external bus enabled devices (Col. 3, lines 24-40). Herzi and Chaiken are analogous art because they both involve providing USB support in BIOS. At the time of the invention, it would have been obvious to one of

ordinary skill in the art to apply Chaiken's periodic interrupt to Herzi's system. A motivation for doing so would have been to ensure the integrity of the system.

As per claim 2, Herzi teaches the external bus support component is to provide support for external bus enabled devices until an operating system providing external bus support is loaded (Col. 1, line 66 – Col. 2, line 20).

As per claim 3, Herzi teaches the system of claim 1 wherein the external bus enabled devices comprise at least one of a keyboard, a mouse, a floppy drive, a biometric device, a hard disk drive, a compact disk read-only memory (CD-ROM) player (Fig. 2).

As per claim 4, Herzi teaches the system of claim 1 wherein:

the external bus controller is a Universal Serial Bus (USB) host controller (Claim 7);

the external bus support component is a USB support component (Fig. 4); and

the external bus enabled devices are USB devices (Claim 8).

As per claim 6, Chaiken teaches the processor conforms to the 32 bit Intel Architecture (IA-32) and the periodic interrupt is a system management interrupt (SMI) (Col. 3, lines 24-40; Col. 2, lines 6-19).

'As per claim 7, Chaiken teaches the processor is compatible with the 32 bit Intel Architecture (IA-32) (Col. 2, lines 6-19).

As per claim 8, Herzi teaches a system comprising:

a processor coupled to a bus (Fig. 2, CPU 201);

a memory coupled to the bus (Fig. 2, memory 203);

an external bus controller coupled to the bus (Fig. 1, USB controller; Col. 2, 24-35);

an external bus enabled device coupled to the external bus controller (Fig. 1, USB keyboard, USB mouse);

a basic input-output system (BIOS) coupled to the bus (Fig. 2, BIOS 202), the BIOS having instructions which when executed cause the processor to perform operations comprising:

obtaining a portion of the memory to be used to maintain a plurality of external bus device data (Col. 6, lines 16-33);

causing an interrupt to be generated (Figs. 3 & 5); and

handling input produced by the external bus enabled device using the portion of the memory responsive to the interrupt (Figs. 3 & 5).

However, Herzi does not expressly teach generating the interrupt periodically. Chaiken teaches generating a periodic interrupt and providing support for external bus enabled devices (Col. 3, lines 24-40). Herzi and Chaiken are analogous art because they both involve providing USB support in BIOS. At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Chaiken's periodic interrupt to Herzi's system. A motivation for doing so would have been to ensure the integrity of the system.

As per claim 9, since Herzi/Chaiken teaches the system of claims 6 and 8, Herzi/Chaiken teaches the claimed system.

As per claim 11, Chaiken teaches de-allocating a portion of memory when the operating system is loaded (Col. 1, line 60 – Col. 2, line 5).

As per claim 12, since Herzi/Chaiken teaches the system of claims 4 and 8, Herzi/Chaiken teaches the claimed system.

As per claims 14, 15, 17 and 19, since Herzi/Chaiken teaches the system of claims 8, 9, 11, and 12, Herzi/Chaiken teaches the claimed method.

As per claims 24, 25, 27, and 28, since Herzi/Chaiken teaches the system of claims 8, 9, 11, and 12, Herzi/Chaiken teaches the claimed medium.

3. Claims 5, 13, 18, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi/Chaiken as applied to claims 1, 8, 14, and 24 above, and further in view of Intel, "Instantly Available Power Managed Desktop PC Design Guide", Revision 1.2, September 25, 1998 ("Intel").

As per claim 5, Chaiken teaches adherence to the ACPI specification (Col. 5, lines 8-13 & 56-64), but does not expressly teach details of memory mapping and BIOS with regards to the ACPI specification and the BIOS comprises a software component to implement the ACPI specification. Intel teaches such details (Sec. 4, ACPI BIOS design considerations). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Intel's ACPI implementation to Herzi/Chaiken's system. A motivation for doing so would have been to facilitate power management (Intel, Sec. 1.1).

As per claims 13, 18, and 29, Intel teaches a non-volatile-sleeping (NVS) memory region (Sec. 4.2.2, ACPI Non-Volatile-Sleeping Memory).

4. Claims 10, 16, 22, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi/Chaiken as applied to claims 8, 14, and 24 above, and further in view of Abgrall, U.S. Patent No. 6,401,202.

As per claims 10, 16, 22, and 26, Herzi/Chaiken does not expressly teach the details of disabling the periodically generated interrupt when an operating system providing external bus device support is completely loaded. Abgrall teaches disabling an interrupt once a task has been completed (Fig. 6, step 650). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Abgrall's disabling an interrupt to Herzi/Chaiken's system. A motivation for doing so would have been to ensure the integrity of the system.

5. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi/Chaiken as applied to claim 14 above, and further in view of Eichler, Jr. et al., U.S. Patent No. 6,772,252 ("Eichler").

As per claims 20 and 21, Chaiken teaches removing code from memory when the code is no longer necessary (Col. 1, line 60 – Col. 2, line 5), but does not expressly teach determining whether an operating system providing USB device support is loaded. Eichler teaches determining whether an operating system provides USB support (Fig. 7, step 704). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Eichler's determining to Herzi/Chaiken's method. A motivation for doing so would have been to determine when code is no longer necessary.

6. Claims 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi/Chaiken as applied to claim 14 above, and further in view of Gentry, Jr. et al., U.S. Patent No. 6,467,008 ("Gentry").

As per claim 23, Herzi/Chaiken does not expressly teach adjusting the rate of the interrupt based on data traffic involving the one or more USB devices. Gentry teaches adjusting the rate of an interrupt based on data traffic (Col. 7, line 51 – Col. 8, line 11) involving one or more USB devices (Col. 5, lines 53-65). At the time of the invention it would have been obvious to one of ordinary skill in the art to apply Gentry's interrupt modulation to Herzi/Chaiken's method, in order to allow a processor to be more responsive to other tasks (Gentry, Col. 7, lines 19-36).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. After the move in October, the new telephone number will be 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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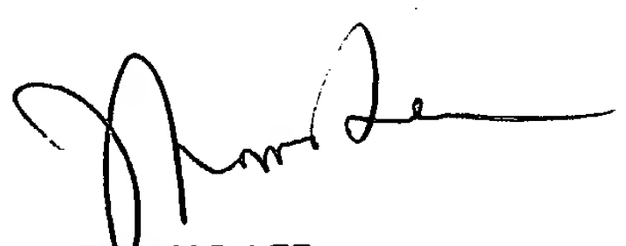
August 30, 2004



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